

## EVLDO2 Evaluation Board For The IXLDO2 Ultra High Speed Laser Diode Driver IC.

### Introduction

The IXLDO2 laser diode driver is designed to drive single junction laser diodes in a differential fashion. This technique provides the highest possible slew rate across the diode. The IXLDO2 is capable of currents exceeding 2A, an operating frequency of 17MHz, a minimum pulse width of <1.5nS and a rise time of approximately 600pS. In addition the pulse width and the current programming can be modulated in real time to >10MHZ.

The EVLDO2 is a fully loaded and tested circuit board available from DEI. The EVLDO2 includes the IXLDO2 laser diode driver IC and associated circuitry required to operate the IXLDO2.

**Note:** The EVLDO2 is intended to be used as *evaluation* module, to demonstrate the use of the IXLDO2 and as a development tool for the engineer designing with the IXLDO2. The EVLDO2 is **not** intended to be a general use, OEM, “turn-key” or “drop-in” *application* module. Due to the wide variety of laser diode packages and associated lead inductances, we simply cannot guarantee satisfactory performance for **all** laser diode packages. Therefore, the board layout has been minimized to utilize a single diode package to reduce parasitic inductance as much as possible. It is up to the end user to obtain acceptable performance when adapting cables, strip-lines, or any other diode package beyond what the board was designed for.

This technical note covers the features and operation of the EVLDO2 evaluation board and the IXLDO2 driver IC.

# **\*\*Caution\*\***

The following precautions must be taken to prevent damage to the IXLDO2SI

**\*\* Do not physically tie the PDN J1 continuously high. Do not gate the PDN input high for long periods of time. The PDN gate signal must be removed (held low) at the end of the FIN pulse train. The complementary outputs of the IXLDO2 are active when PDN is high, drawing current continuously\*\***

**\*\* Do not exceed total power dissipation of 3 Watts. (See Gate Timing and Duty Cycle and Power Dissipation sections of this technical note.) \*\***

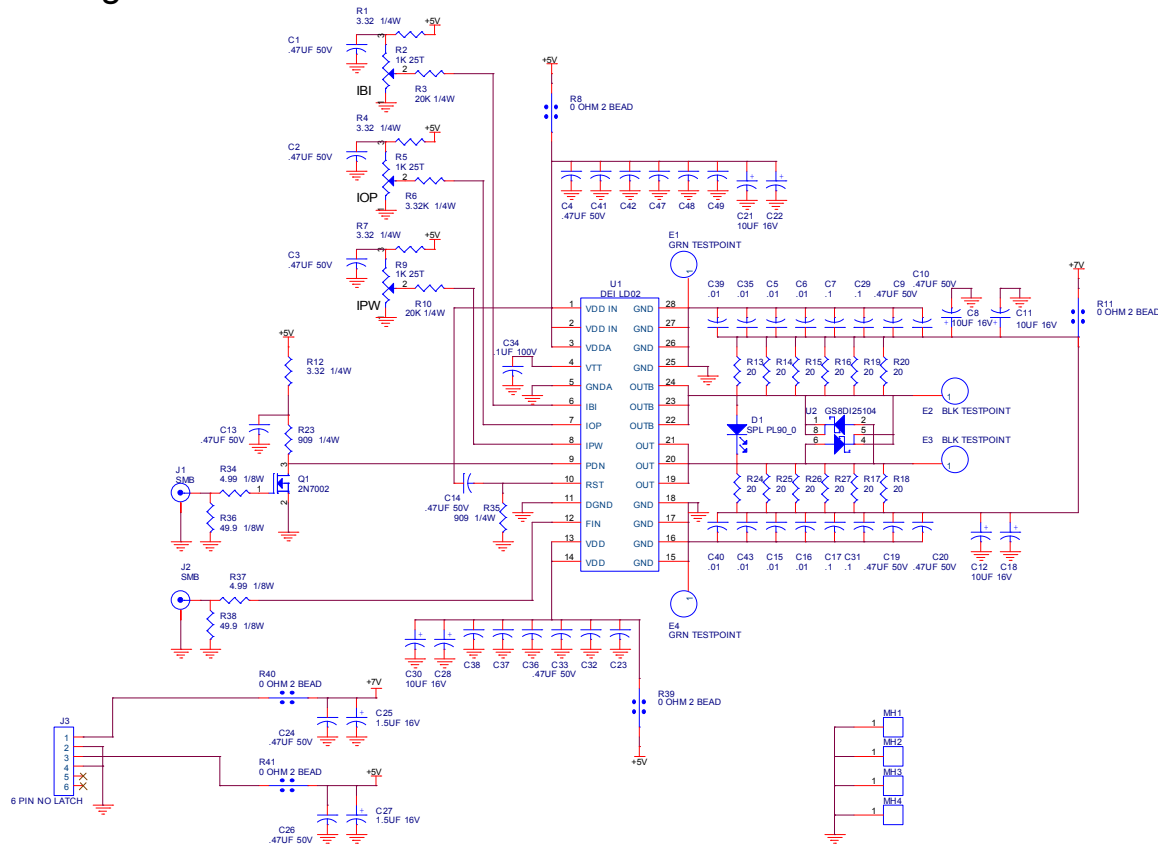
**\*\* Do not exceed 7VDC on J3 pin 1. \*\***

<b>J1</b>	<b>PDN</b>
<b>J2</b>	<b>FIN</b>
<b>J3 Pin 1</b>	<b>7V Max</b>
<b>J3 Pin 2</b>	<b>Ground</b>
<b>J3 Pin 3</b>	<b>5V</b>
<b>J3 Pin 4</b>	<b>Ground</b>
<b>J3 Pin 5</b>	<b>N/C</b>
<b>J3 Pin 6</b>	<b>N/C</b>

**Table 1 Input Connections**

## EVLDO2 Circuit Diagram

The circuit diagram for the EVLDO2 evaluation PCB is shown in Figure 1.



**Figure 1 PCB Schematic**

Referring to Figure 1, the input to J1 is the Power Up command (PDN). Q1 is an inverter to allow the proper function of the PDN at pin 9 of the IXLDO2. When power is applied to J3 of the EVLDO2, the PDN (pin 9) is pulled up to the +5V supply, deactivating the IC. A positive PDN gate signal at J1 is required to activate the IC.

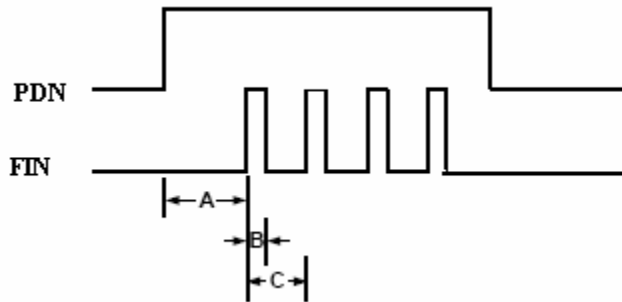
The frequency input signal or pulse command is applied to J2 (FIN). This is a 3V to 5V into 50 Ohm positive-going gate. The output pulse width is controlled by the current applied to pin 8 (IPW) of the IXLDO2 via R9 and R10, not the width of the gate signal applied to J2. The IOP, pin 7 of the IXLDO2, is used to set the peak output current. This current is set via R5

and R6. The IBI input to pin 6 of the IXLDO2 is typically set to 100uA. This current is supplied via R2 and R3.

The bypassing of the Vdd and the +7V power is very critical. This bypassing can also vary dependent on the pulse width and the frequency of operation. The capacitors used as bypassing must have low series inductance and low series resistance to insure the high speed performance of the IXLDO2.

### Gate Timing

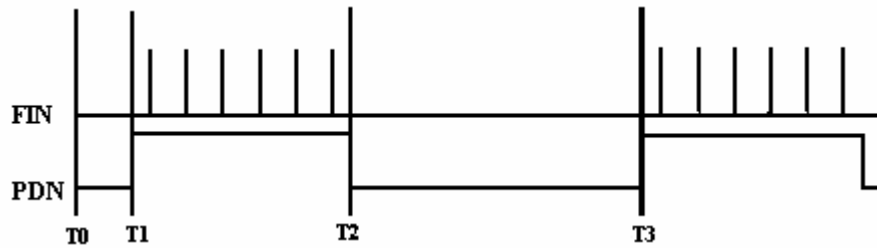
The proper gate timing of the IXLDO2 is extremely critical. The device is capable of 2A of output current and may consume in excess of 3A during the pulse. If the supply voltage is at 7V with 3A of current the total power dissipated is 21W, far beyond the heat sinking capability of the evaluation board. Therefore unless additional heat sinking of the IXLDO2 is provided, the duty cycle must be limited to a total power dissipation of 3W. This would indicate a 14% maximum full power duty cycle.



**Figure 2 Control Gate Timing Diagram**

The Power Up gate signal (PDN) J1 is applied to activate the device. Time interval “A” is the delay between the rising edge of the PDN and the FIN J2 control gate signal. This delay should be approximately 30nS. Time interval “B” is the pulse width of the control gate which has a range of 1nS to several microseconds. The maximum frequency  $1/C$  is approximately 17MHZ. To avoid over heating the IXLDO2SI the PDN should be removed (held low) at the end of the FIN pulse train.

## Duty Cycle And Power Dissipation



**Figure 3 Duty Cycle**

Figure 3 illustrates the Duty Cycle, FIN, and PDN relationship. The PDN must stay in a TTL high state for the duration of the laser light burst, T1 to T2.

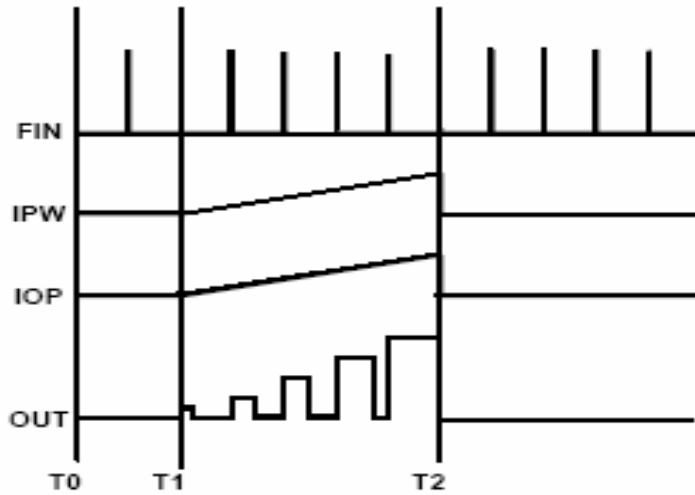
The Duty Cycle is defined as:  $DC = T2 - T1 / T3 - T1$

Power in the IC is defined as: Total dc power x Duty Cycle.

With the limited heatsinking of the IXLDO2 provided by the EVLDO2 evaluation board, the maximum full power duty cycle should be limited to  $DC = 0.14$  or 14%.

### Modulation

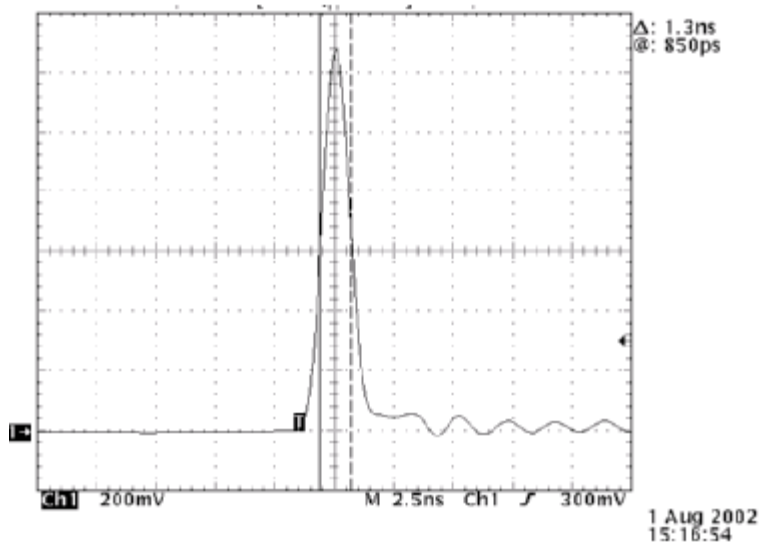
Figure 4 illustrates the simultaneous modulation of both the IPW control current and the IOP control current. The FIN frequency in this figure is held constant. At T0 the IPW and the IOP signals are near zero. Both begin to ramp up at T1 and reach their maximums at T2. As illustrated, the output current rises in amplitude with the increasing of IOP and the pulse width widens with the IPW ramp. An additional modulation can be added to the two by also modulating the frequency of the FIN signal. This will allow three modes of simultaneous modulation. The three modes do not have to be used together, each is fully independent. The obvious caveat is that the pulse width must be consistent with the chosen frequency. This agility provides the designer with a broad range of design choices.



**Figure 4 IPW and IOP Modulation**

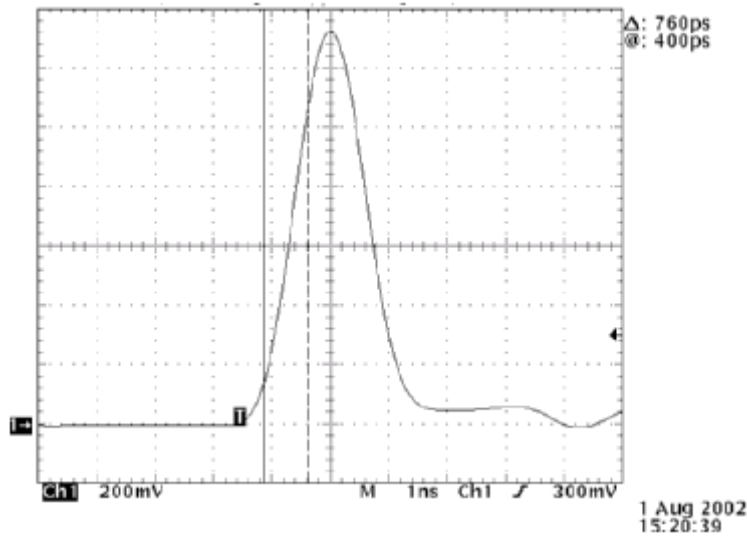
**Device Performance**

Figure 5 illustrates the optical pulse generated driving an Infineon SPLPL90\_0 laser diode. The optical pulse is detected with a Melles Griot model 13DAH0003 photo detector. The optical waveform measured Full Width Half-Max (FWHM) is 1.3nS.

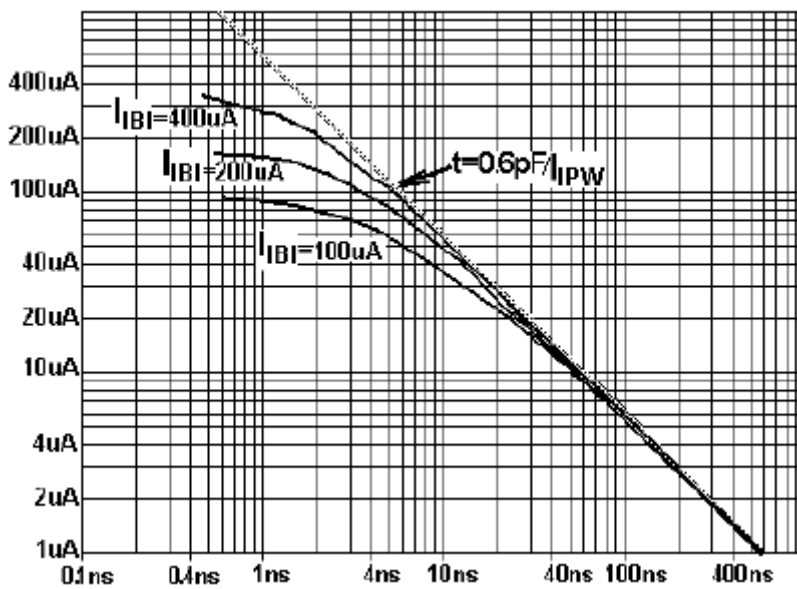


**Figure 5 Output Optical Pulse**

In Figure 6 we see the pulse rise time of approximately 760pS. System jitter was measured at <300pS.



**Figure 6 Pulse Rise Time**



**Figure 7 Output Pulse vs. Programming Current**

Figure 7 is an illustration of the pulse width vs. programming current. Adjusting potentiometer R9 on the evaluation board varies the programming current. However, the programming current could just as well be a time varying signal. The bandwidth of this portion of the IXLDO2 is equivalent to the maximum operating frequency of 17MHz. For the fastest response time of a dynamic signal this pin should be driven from a low source impedance.

The following pin description table is for the IXLDO2 device, not the evaluation board.

Table 1 IXDLO2 Pin Description

Pin	Name	Description
1,2,13, 14	VDD	This pin is a high current, low inductance pin designed to accept peaks of 2A at 5V.
3	VDDA	This is a low current analog power input. Circuit components sensitive to the noise present on VDD are supplied by this pin.
4	VTT	This pin is the $\frac{1}{2}$ VDDA internal analog comparator reference point.
5	GND A	Low current, low noise analog return. Noise sensitive circuit components are returned here.
6	IBI	The $I_{IBI}$ current flowing into the IBI pin acts as a baseline current with respect to the $I_{IPW}$ current to compensate for internal delays.
7	IOP	The $I_{IOP}$ current flowing into the IOP pin programs the laser diode output switches, pins 19 – 24. The program ratio is 1:1000X. This means a 1mA current will produce 1A.
8	IPW	The $I_{IPW}$ current flowing into the IPW pin determines the output current pulse width, $t_{PW}$ , with respect to $I_{IBI}$ . If $I_{IPW} = I_{IBI}$ , the pulse width is 0. As $I_{IPW}$ approaches $I_{IBI}$ but is less than $I_{IBI}$ , the pulse width becomes non-zero.
9	PDN	A TTL high on this pin will power down the device so that only leakage current will flow from VDD to DGND. A TTL low will turn on the device within 30ns.
10	RST	The system reset pin that initializes the device so that it starts in a predetermined initial state.
11	DGND	This pin is the return for the input logic, $I_{IBI}$ , $I_{IOP}$ , and $I_{IPW}$ currents. It is internally connected to the other grounds, GND A and GND, through the substrate.
12	FIN	With PDN low, a positive edge of a TTL compatible signal here will produce the pulse current output available at the OUT and the complement of it at OUTB pins.
15,16,17,18,25,26,27,28	GND	Output ground pins designed for low inductance.
19,20,21	OUT	True laser diode drive output current. Designed for low inductance and output voltage compliance to +7V.
22,23,24	OUTB	Complementary laser diode drive output current. Designed for low inductance and output voltage compliance to +7V.

With respect to pin 7, the programming of this node is via R5 on the evaluation PCB. However, the programming signal could also be a time varying signal. The bandwidth of this input on the IC is approximately 10MHz.

For additional information on the IXLDO2, including operating parameters, functional block diagram and package drawing, see the IXLDO2 datasheet.